# MT6223(P) Phone Design Notice

***2007/07/03***

***WCP/SA/RP1***


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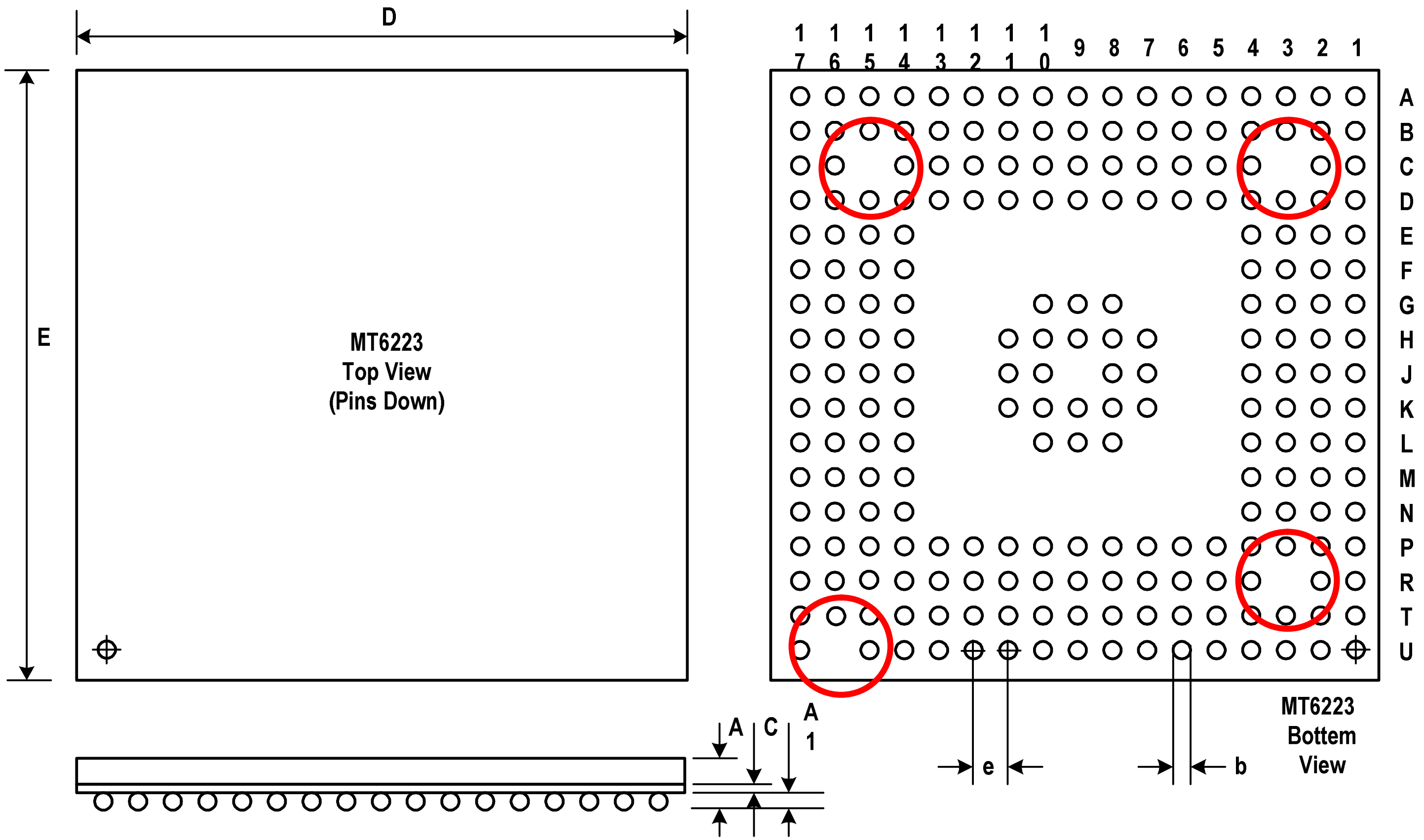
# MT6223 Package




| Body Size | | Ball Count | Ball Pitch | Ball Dia. | Package Thk. | Stand Off | Substrate Thk. |
|---|---|---|---|---|---|---|---|
| D | E | N | e | b | A (Max.) | A1 | C |
| 9.0 | 9.0 | 224 | 0.5 | 0.275 | 1.2 | 0.21 | 0.36 |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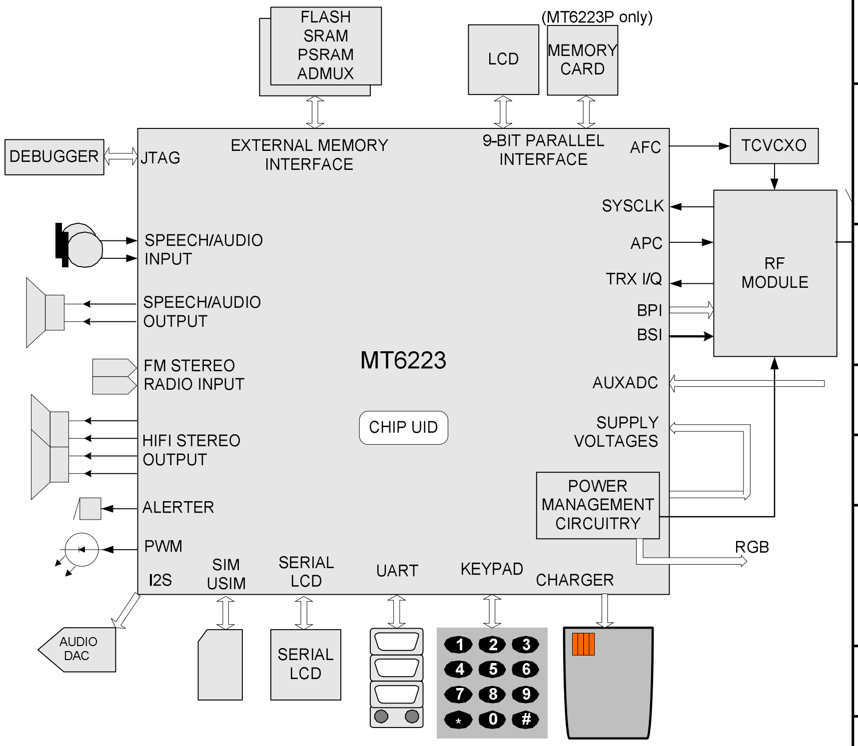
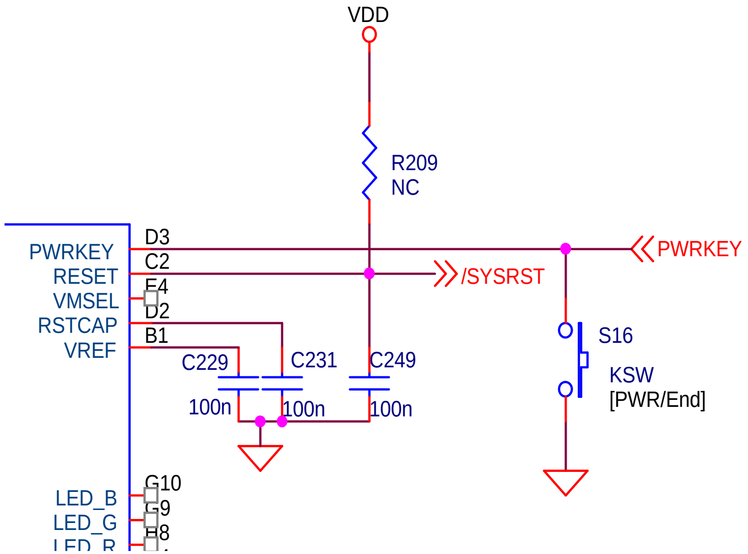
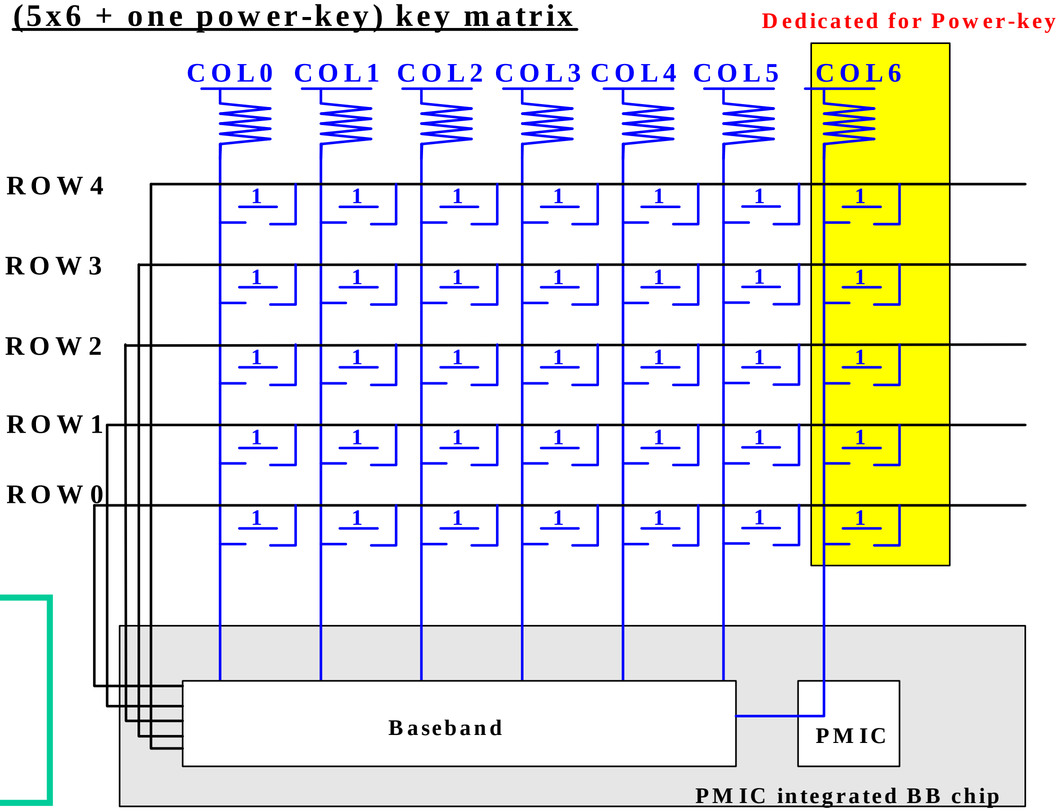
# MT6223 vs MT6205




| | | MT6205B | MT6223 |
|---|---|---|---|
| LCM I/F | Parallel I/F | X | 8/9-bit |
| | Serial I/F | V | V |
| FM Radio | Input | X | Stereo |
| | Recording | X | Mono |
| Audio DAC | Channel | X | 2 |
| | Resolution | X | AC |
| I2C | | X | V |
| I2S | | X | V |
| BT | Voice Link | X | DAI/PCM |
| | Audio Link | X | I2S |
| EINT | | X | 4 |
| Keypad | | 5x5 | 5x6 |
| UART | | 2 (115.2kbps) | 3 (921.6kps) |
| ADC | | 5 | 3(ext)+4(int) |
| SW Card | | X | MT6223P only |

# Keypad




- MT6223 is 5x6 matrix
- **COL6** is dedicated for POWER_KEY (internal connection).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# ADC

| ADC channel | Function | Pin out |
| --- | --- | --- |
| AUXADC_0 | External ADC channel | M2 |
| AUXADC_1 | External ADC channel | M3 |
| AUXADC_2 | External ADC channel | N2 |
| AUXADC_3 | Internal reference voltage | x |
| AUXADC_4 | ADC for **Charger voltage detection** | x |
| AUXADC_5 | ADC for **charging current sense** | x |
| AUXADC_6 | ADC for **Battery Voltage detection** | x |
| AUXADC_7 | Auxiliary ADC channel 0 data register for TDMA event 0 | x |


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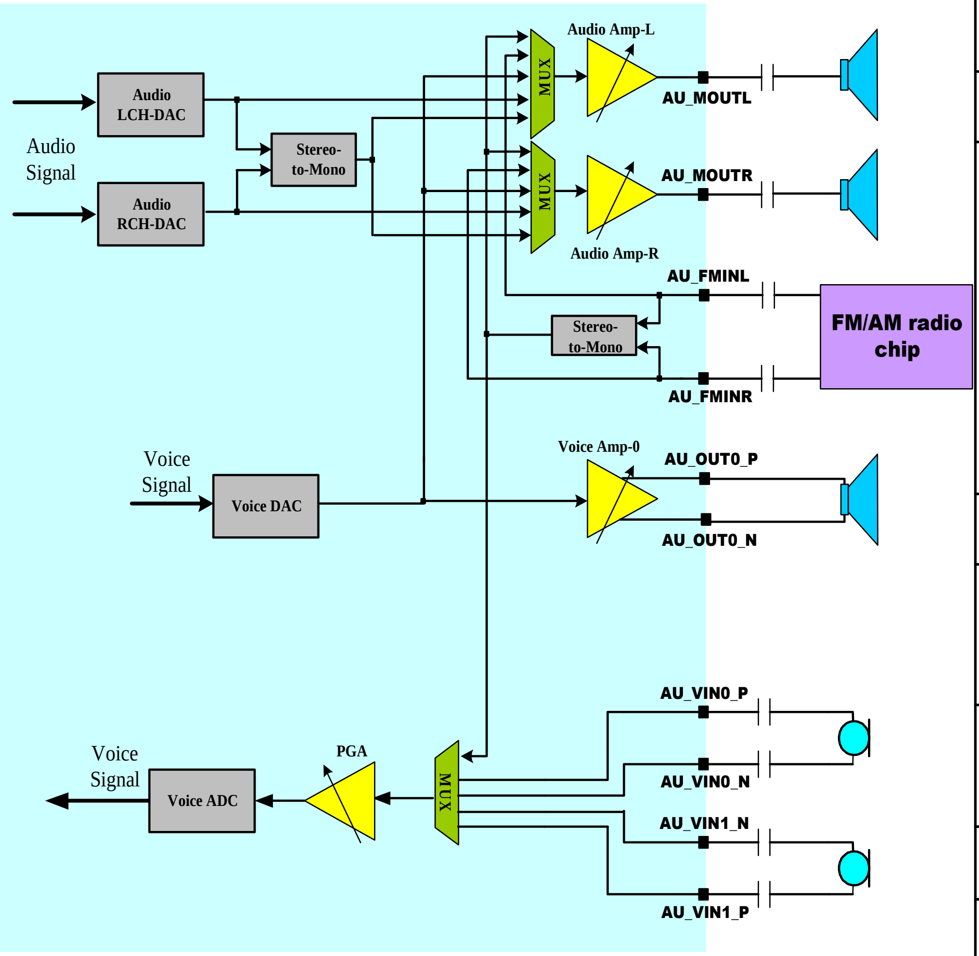
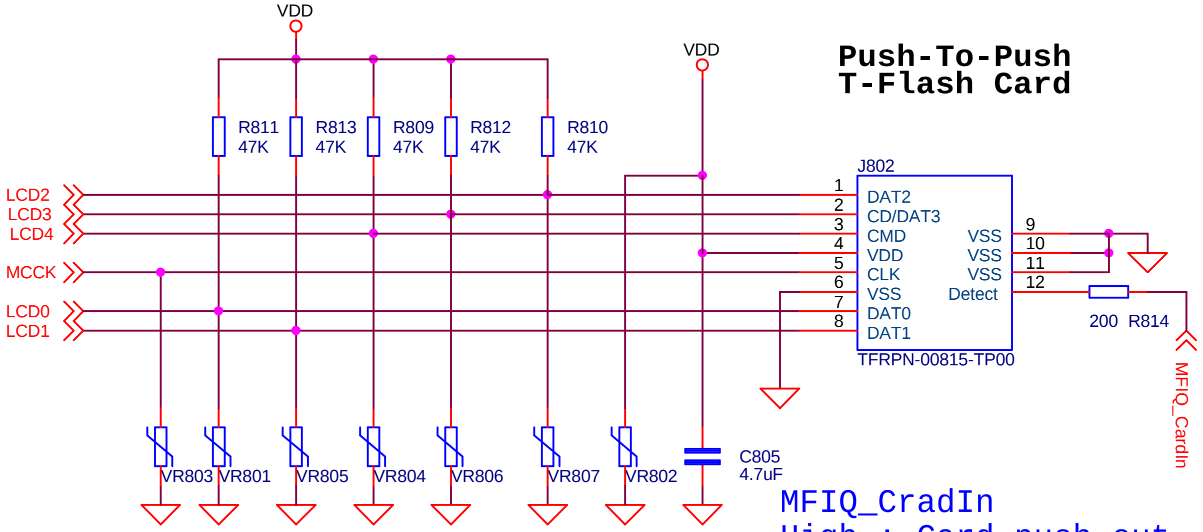
# MT6223 Speech & Audio




| Features | | MT6205 | MT6223 |
|---|---|---|---|
| DSP | | 1 | 2 |
| Speed | | 52MHz | 104MHz |
| Speech Codec | FR | V | V |
| | HR | V | V |
| | EFR | V | V |
| | AMR FR | X | V |
| | AMR HR | X | V |
| CTM | | X | V |
| Noise Reduction | UL | X | V |
| | DL | X | V |
| Noise Suppression | | X | V |
| Echo Cancellation | | X | V |
| Echo Suppression | | V | V |
| VR | | X | V |
| MP3 | | X | V |
| WT 64Tones | | X | V |

# LCD & Memory Card I/F

| LCD IO | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Parallel IF | PD8 | PD7 | Pd6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Serial IF | SCLK | SDA | SA0 | | | | | | |
| MSDC IF | | | | | MCCM | MCDA 3 | MCDA 2 | MCDA 1 | MCDA 0 |

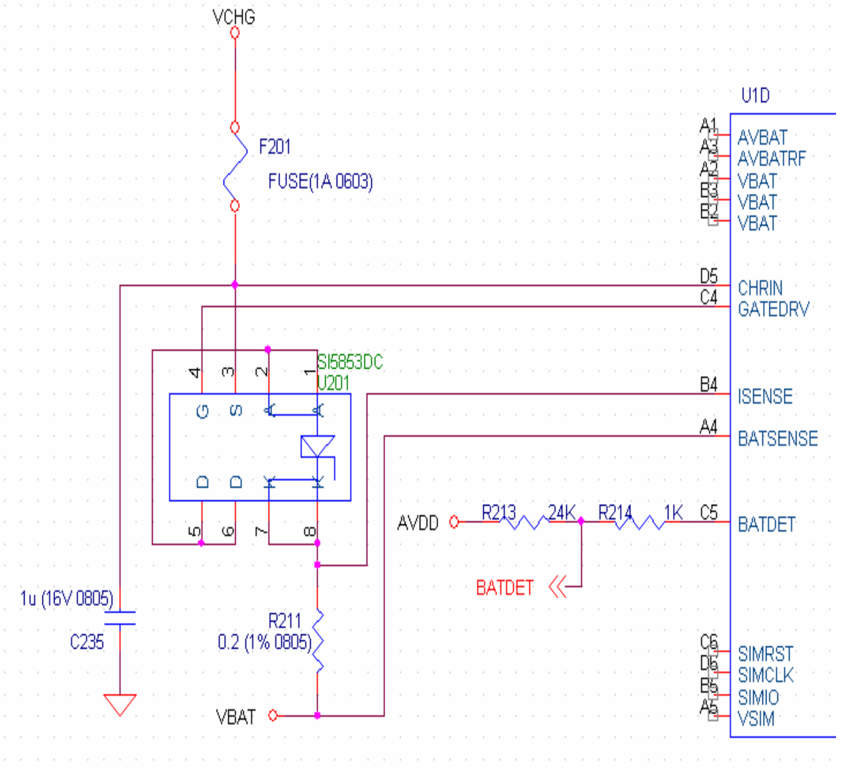



MFIQ_CradIn
High : Card push out
Low : Card push in

- LCD I/F can control 2 LCMs and 1 memory card at the same time.
- Memory Card I/F is **MT6223P** only.
- For SW memory card, if EINT is exhausted, it could uses MFIQ for Card detection. Anyway MFIQ acts when 26MHz system clock on.

# PMU of MT6223

## 1.1 Charger Schematics




| | MT6305B | MT6318 | MT6223 |
|---|---|---|---|
| 1 | CHRIN | AC | CHRIN |
| 2 | GATEDRV | GDRVAC | GATEDRV |
| 3 | ISENSE | ISNENSE | ISENSE |
| 4 | BATSNS | VBAT | BATSENSE |
| 5 | BATDET | BAT_ON | BATDET |
| 6 | CHRCNTL | X (Through SPI) | X (Internal) |
| 7 | CHRDET | INT | X (Internal) |
| 8 | BATUSE (Li-ion and NiMH) | X (Only Li-ion) | X (Only Li-ion) |
| 9 | X (Share with CHRIN) | USB | X (Share with CHRIN) |
| 10 | X (Share with CHRIN) | GDRVUSB | X (Share with CHRIN) |
| 11 | X (External Resistor) | VB_OUT | X (Internal) |
| 12 | X (External Resistor) | ISENSE _OUT | X (Internal) |
| Total | 8 | 10 | 5 |

# PMU of MT6223

## 1.2 Charger Current

| | | MT6305B | MT6318 | MT6223 |
|---|---|---|---|---|
| Sense Resistor | | 0.4 Ohm | 0.2 Ohm | **0.2 Ohm** |
| Pre-Charge | | 25 | 62.5 | **62.5** |
| CC | 0 | 400 | 62.5 | **62.5** |
| | 1 | | 90 | **90** |
| | 2 | | 150 | **150** |
| | 3 | | 225 | **225** |
| | 4 | | 300 | **300** |
| | 5 | | 450 | **450** |
| | 6 | | 650 | **650** |
| | 7 | | 800 | **800** |

**For Layout:**
Connect ISENSE and BATSNS directly to the two terminal of sense resistor to get a precise charge current. Don't connect BATSNS to other VBAT trace near IC, which could cause charge current mismatch for over hundreds mA.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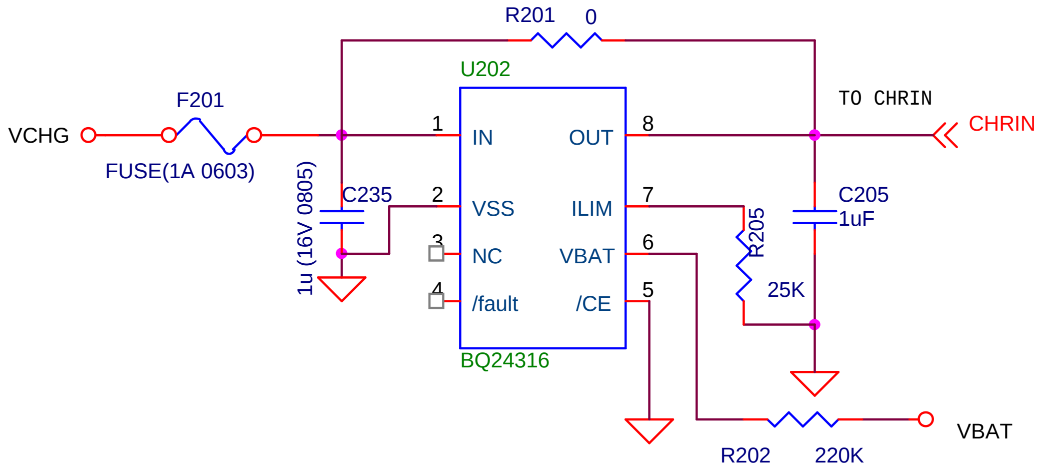
# PMU of MT6223

## 1.3 Charger Protection

| | MT6305B | MT6318 | MT6223 | OVP/OCP |
|---|---|---|---|---|
| Max. Charger Input | 15V | 15V | 9V | 30V |
| Charger OVP Point | 9V | 9V | 7V | 6.8V |

**Ext_OVP/OCP:**



# PMU of MT6223

## 2. LDO

| LDO Current | MT6305B (mA) | MT6318 (mA) | **MT6223 (mA)** |
|---|---|---|---|
| VCORE | 200 | 200 | **200** |
| **VA** | **150** | **150** | **125** |
| VIO | 100 | 100 | **100** |
| **VM** | **150** | **150** | **75** |
| VTCXO | 20 | 20 | **20** |
| VSIM | 20 | 20 | **20** |
| **VRF** | X | X | **250** |
| VRTC | V | V | **V** |
| BAT_BACKUP | X | V | **V** |
| VUSB | X | 20 | X |
| VMC | X | 250 | X |
| VSW_A | X | 50 | X |
| VIBR | X | 200 | X |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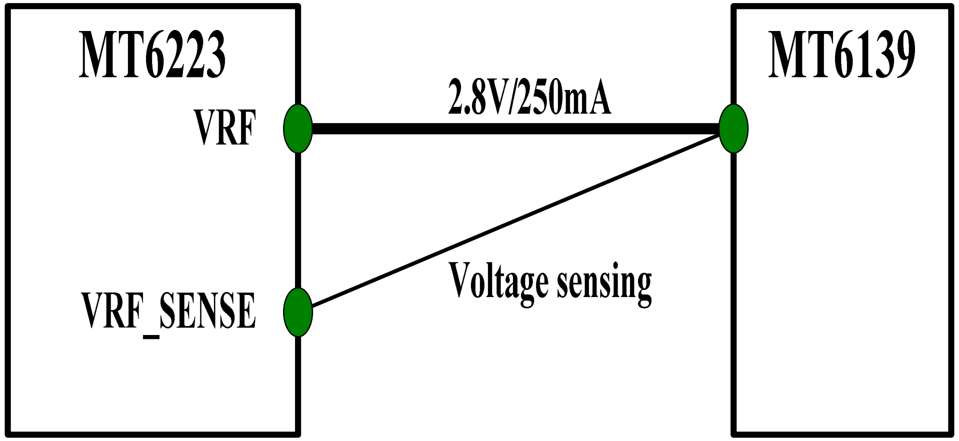
# PMU of MT6223

## LDO-Capacitor Selection

| LDO | VA | VRF | VTCXO | VCORE | VIO | VM | VSIM | VRTC | BAT_ _BACKUP |
|---|---|---|---|---|---|---|---|---|---|
| Output Capacitor | 4.7 uF | 4.7 uF | 1 uF | 2.2 uF | 1 uF | 1 uF | 1 uF | 0.1uF | 0.1 uF |
| | X5R | X5R | X5R | X5R | X5R | X5R | X5R | X5R | X5R |




## VRF_SENSE layout notice

**The VRF_SENSE pin should connect to MT6139's power in pin directly to reduce the voltage drop. And the VRF_SENSE trace should be protected by GND in layout.**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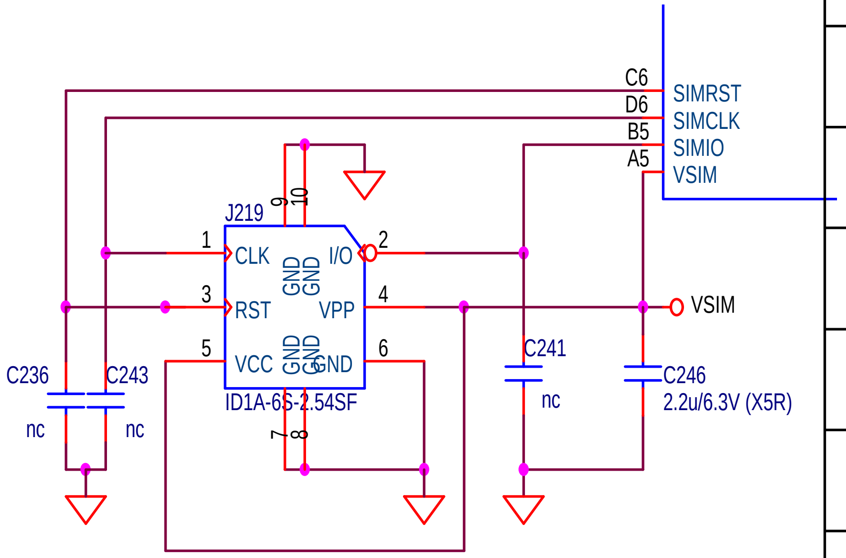
# PMU of MT6223

## 3. SIM




The equivalent capacitor on SIM I/F must be **under 100pF** to insure operation normally.

| | MT6305B | MT6318 | MT6223 |
|---|---|---|---|
| 1 | SIO | SIO | **SIO** |
| 2 | SRST | SRST | **SRST** |
| 3 | SCLK | SCLK | **SCLK** |
| 4 | SIMIO | SIMIO | **X (Internal)** |
| 5 | SIMRST | SIMRST | **X (Internal)** |
| 6 | SIMCLK | SIMCLK | **X (Internal)** |
| 7 | SIMVCC | SIMVCC | **X (Internal)** |
| 8 | SIMSEL | X (Through SPI) | **X (Internal)** |
| Total | 8 | 7 | **3** |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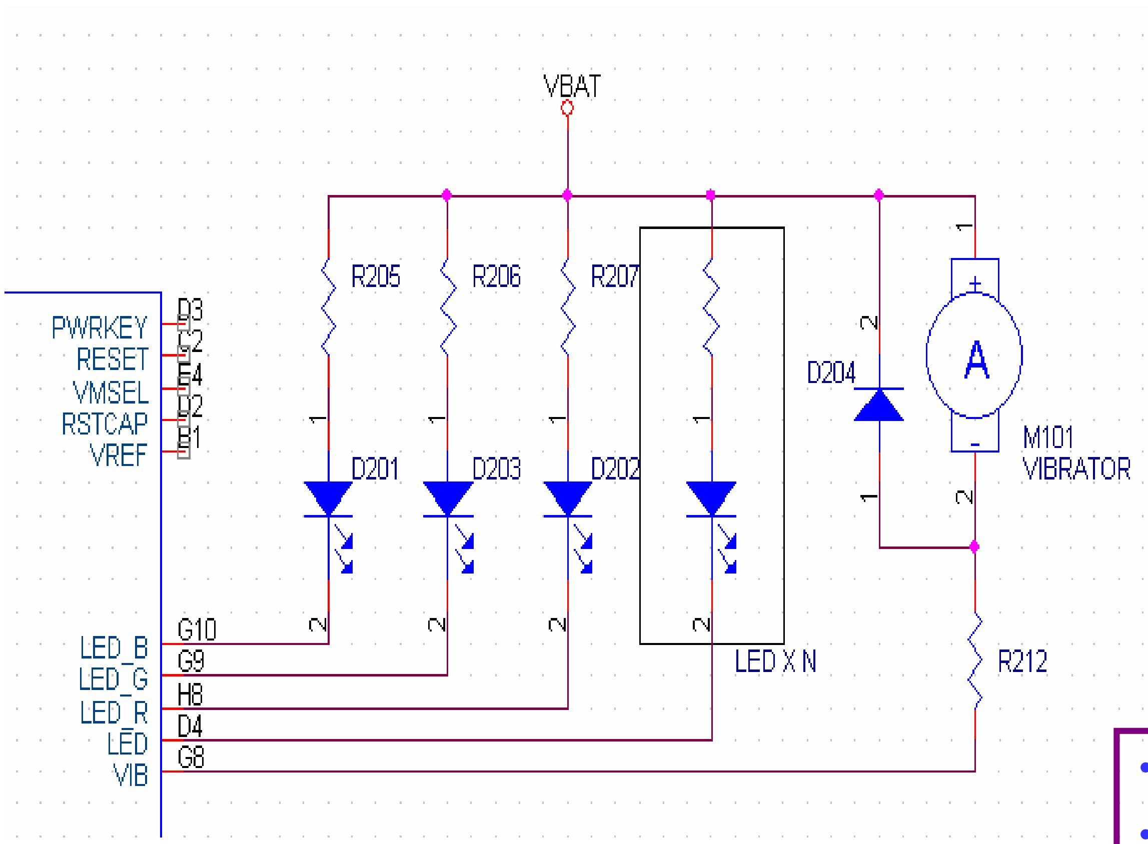
# PMU of MT6223

## 4. LED & Vibrator Driver




| Driver | Current Capability |
| --- | --- |
| LED_R | **25 mA** |
| LED_G | **25 mA** |
| LED_B | **25 mA** |
| LED | 150 mA |
| VIBRATOR | 250 mA |

- **LED with PWM2 control duty cycle**
- **Vibrator/LED_X without PWM**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# VRF Design Note

- Place a 4.7uF X5R capacitor close to PMU to keep stabilization and performance
- Place a 4.7uF X5R capacitor close to RF transceiver to keep stabilization and performance
- Keep VRF trace > 15mil
- Connect sense pin, VRF_SENSE, to RF's power to reduce the voltage drop due to layout and package.
- Protect VRF_SENSE with GND vias and planes.


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# VTCXO Design Note

- Place a 1.0uF X5R bypass cap. and reserve a series 0402 0Ohm near PMU
- Place 1uF X5R//10pF bypass cap. and reserve a series 0402 0Ohm close to TRx pin16 VCCSYN
- Protect VTCXO with GND vias and planes. If RF is on top layer, suggest to put VTCXO routing on layer5 with good GND planes layer4 and layer6
- Do not place any power, analog, digital, and signal traces and vias parallel or close to VTCXO routing.
- Keep VTCXO trace > 15mil
- Do not place VTCXO trace across layers under RF transceiver /Crystal
- Placement of PMU and RF transceiver as close as possible


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# MT6223 Memory Support Plan

<table>
<tr><td colspan="2"></td><td colspan="2">GPRS</td></tr>
<tr><td>NOR</td><td>RAM</td><td>Phone</td><td>Module</td></tr>
<tr><td rowspan="2">64</td><td>16</td><td colspan="2">Intel Crystal (burst, deMux)<br>ST M36W0R6040U3 (64+16 AD MUX, Intel pinout)</td></tr>
<tr><td>32</td><td colspan="2">Intel Crystal (burst, deMux)<br>Spansion PLJ (70/30/16)<br>ST M36W0R6050T1 (64+32 deMux)<br>ST M36W0R6050U0 (64+32 AD MUX)<br>Toshiba TV00560002DDGB (70/30/16)</td></tr>
<tr><td rowspan="2">32</td><td>8</td><td colspan="2">Samsung K5N3208ATM (32+16, ADMUX, Spansion pinout)</td></tr>
<tr><td>16</td><td colspan="2">Intel Crystal (burst, deMux)<br>Spansion NSJ (burst)<br>ST M36W0R5040U3 (32+16 AD MUX, Intel pinout)</td></tr>
</table>

Remark: Spansion VSK, ES at Aug/07, 2008 Q1 MP


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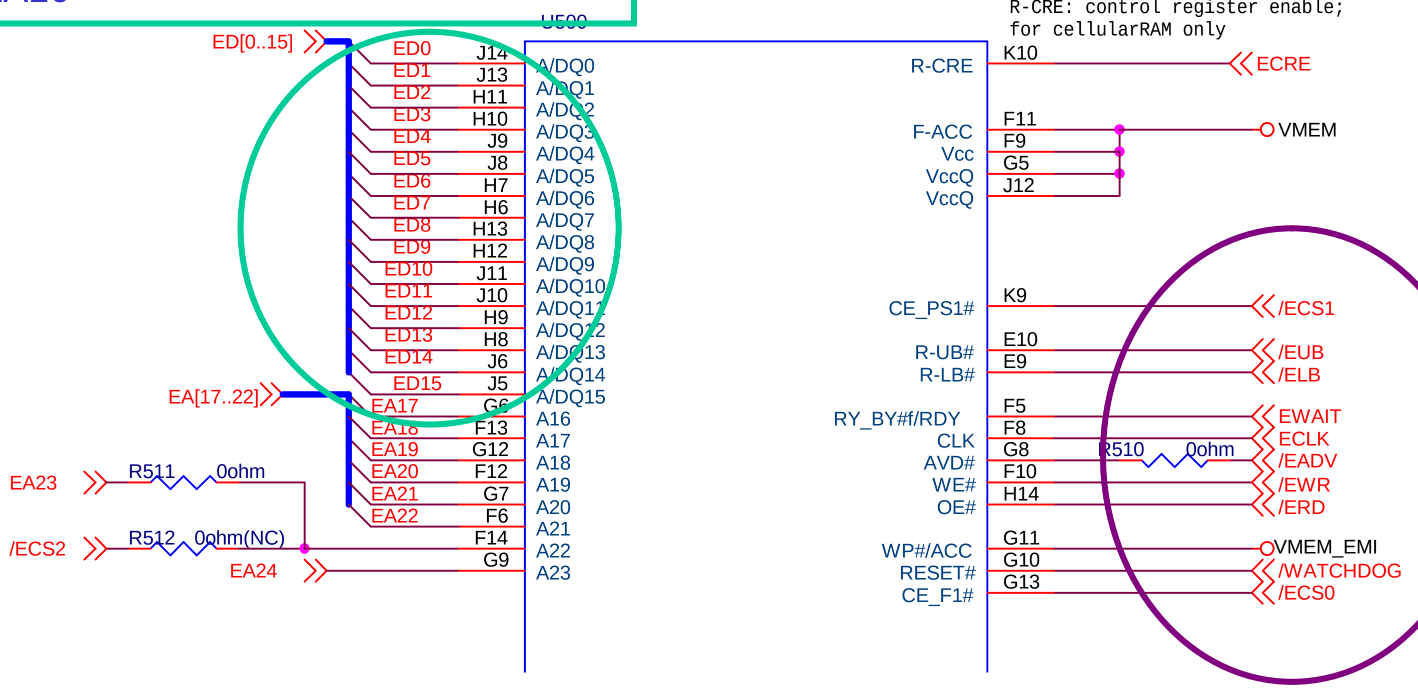
# AD_Mux MCP

For AD_Mux MCP:

1.EA0~15 are share with ED0~15.

2.Baseband's EA17 connect to AD_Mux MCP EA16




Burst mode MCP must check EWAIT, ECLK, and /EADV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# Tools for MT6223

- Flash Tool/ MutilPortDownLoad : Ver_3.1.05
- META : Ver_5.3.8
- ATE : Ver_5.3.8


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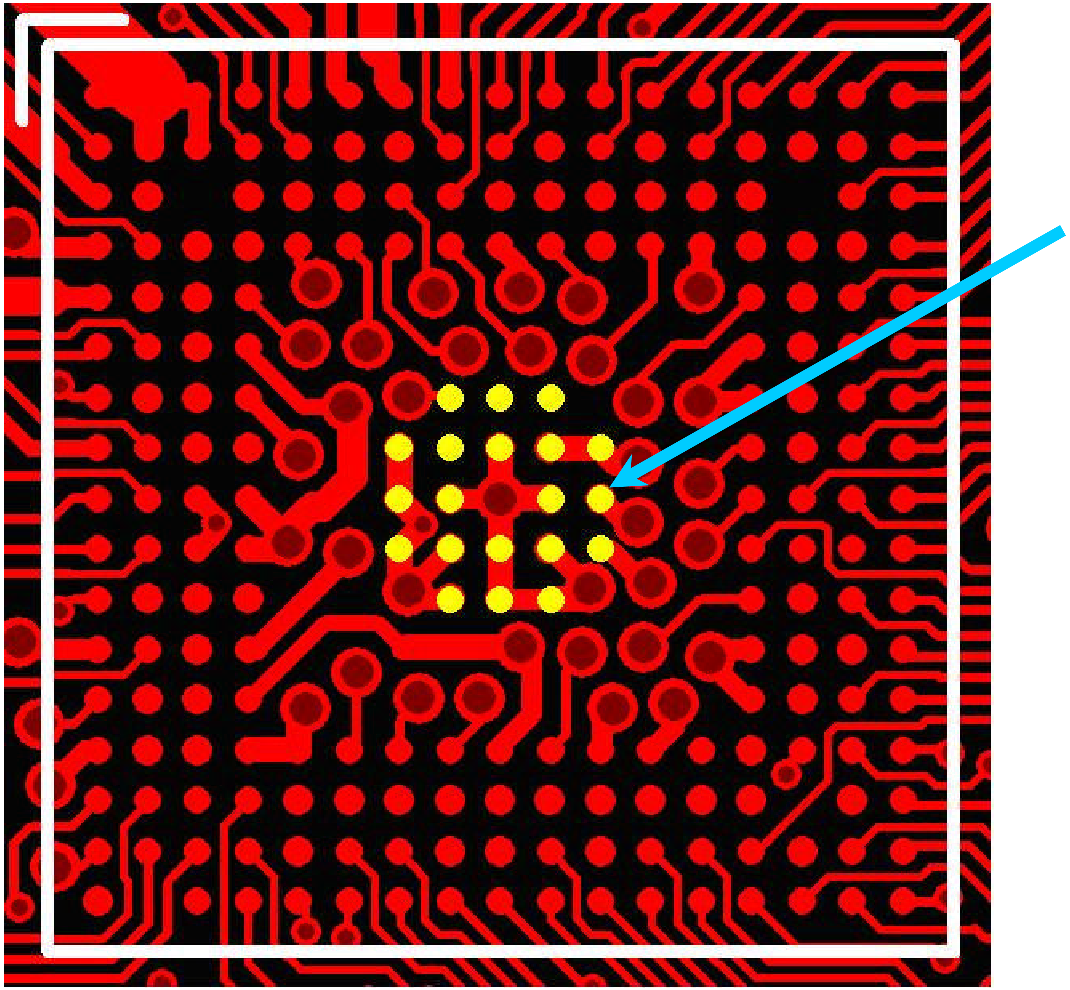
# PCB note_4Layer-I



- MT6223 0.5mm Pitch，top layer 的trace在ball與ball之間必需要使用到3mil/3mil (線寬/線距)，當走出chip時,就要用4mil/4mil (線寬/線距)；雷射孔4/12 mil (Drill/Diameter)。
- 內圈ball：優先使用1-4層貫孔，走內層，因內圈大多是GND pin，建議要配合1-2層雷射孔一起使用。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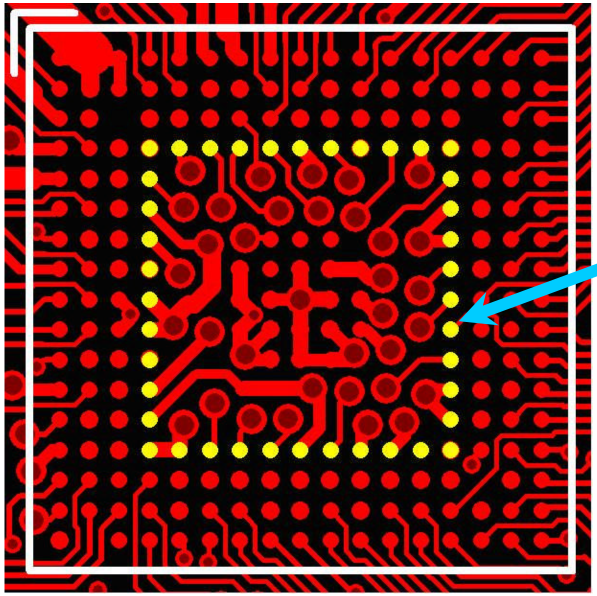
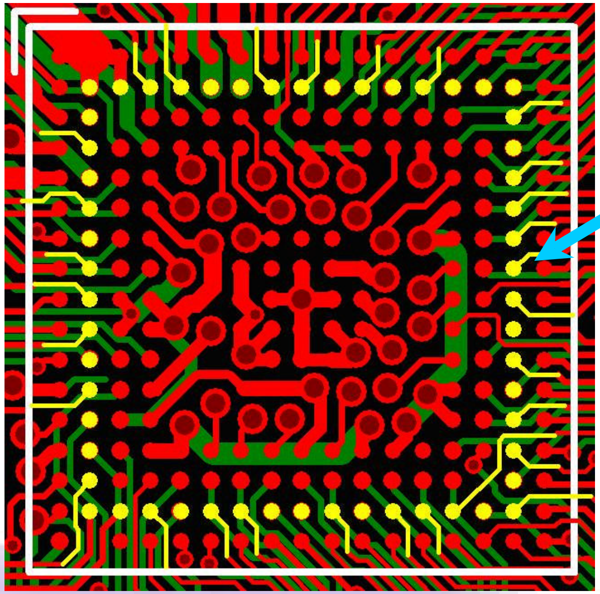
# PCB note_4Layer-II

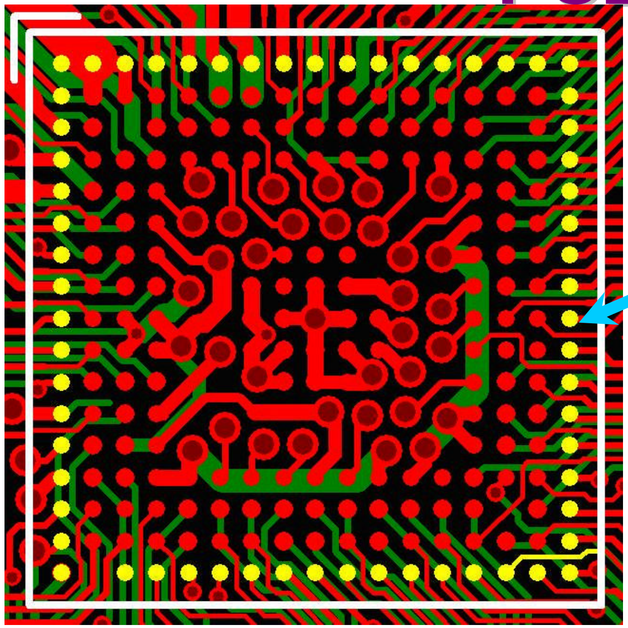


**第4 圈ball：第一優先使用1-4層貫孔，走內層。第二是使用1-2層雷射孔走L2層。**

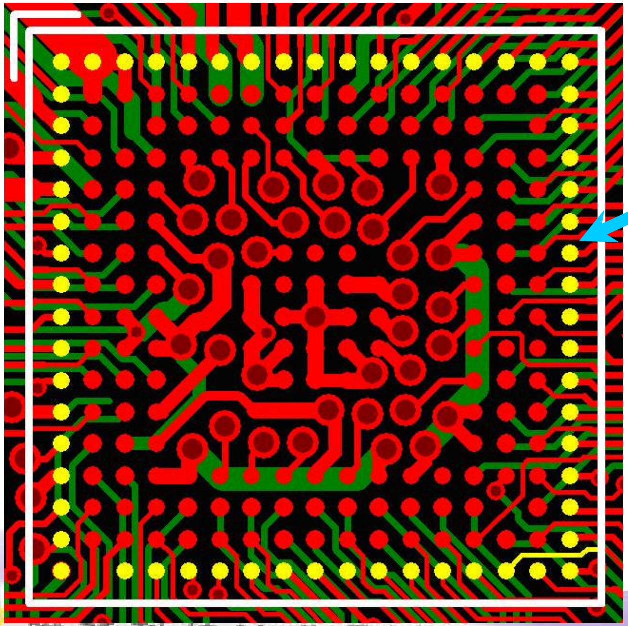


第3圈ball：第一優先使用1-2層雷射孔走L2層。第二是，若內圈有空間，可使用1-4層貫孔，走內層。若TOP走線有穿過ball，線寬與線距就要3mil。

# PCB note_4Layer-III



第2圈ball：第一優先使用3mil線寬的TOP走線，第二才是使用1-2層的雷射孔，走L2層。若TOP走線有穿過ball，線寬與線距就要3mil。



第1圈ball：第一優先使用4mil線寬的TOP走線，第二才是使用1-2層的雷射孔，走L2層。若TOP走線有穿過ball，線寬與線距就要3mil。

**6-layer**

每圈ball的走線方式，大致與 4-layer相同，因6-layer會多埋孔，所以不同在於第4圈及內圈會以1-2層雷射孔加2-5層埋孔爲主。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